WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor integrated circuit comprising:

providing a semiconductor substrate having a fuse device present at least partly in a semiconductor region on or over a surface of the semiconductor substrate;

forming an interlayer insulating film over the surface of the semiconductor substrate, the interlayer insulating film having a top surface;

forming a contact hole in the interlayer insulating film over the semiconductor region such that a columnar insulator region having a top end lower than the top surface of the interlayer insulating film is formed in a central portion of the contact hole; and

forming an electrode in the contact hole such that the electrode contacts the semiconductor region at a periphery of a bottom of the contact hole where the columnar insulator region is not formed.

2. The method according to claim 1, wherein the forming of the contact hole includes:

removing the interlayer insulating film from the periphery of the contact hole while leaving the interlayer insulating film at the central portion of the contact hole;

forming a mask over the interlayer insulating film that exposes the contact hole; and

isotropically etching, through the mask, the interlayer insulating film left at the central portion of the contact hole to make the columnar insulator region have a tapered head with the top end lower than of the top surface of the interlayer insulating film.

3. The method according to claim 2, wherein the isotropically etching further etches the interlayer insulating film around a perimeter of the contact hole to taper the contour of the contact hole.

4. The method according to claim 1, wherein:

the providing of the semiconductor substrate provides the semiconductor substrate further having a second device formed in a second semiconductor region on or over the surface of the semiconductor substrate;

the forming of the contact hole further includes forming a second contact hole in the interlayer insulating film over the second semiconductor region, forming plugs in the contact hole and in the second contact hole and selectively removing the plug from the contact hole; and

the forming of the electrode further includes forming a second electrode that contacts the second semiconductor region via the plug.

5. The method according to claim 4, wherein the forming of the electrode further includes forming a metal film over the interlayer insulating film and patterning the metal film to form the electrode and the second electrode.

6. The method according to claim 1, wherein, within the contact hole, a ratio of an area where the insulator region does not exist to a total area of the bottom of the contact hole is within a range of from about 0.2 to about 0.5.

7. A semiconductor integrated circuit comprising:

a semiconductor substrate having a fuse device present at least partly in a semiconductor region on or over a surface of the semiconductor substrate;

an interlayer insulating film covering the surface of the semiconductor substrate, the interlayer insulating film having a top surface and a contact hole over the semiconductor region, a central portion of the contact hole having a columnar insulator region having a top end lower than the top surface of the interlayer insulating film; and

an electrode that contacts the semiconductor region at a periphery of a bottom of the contact hole.

8. The semiconductor integrated circuit according to claim 7, wherein the electrode is formed of a film primarily composed of a flowable metal that flows into the semiconductor region through an interface at the bottom of the contact hole.

9. The semiconductor integrated circuit according to claim 7, wherein the electrode is made of a film of aluminum or an aluminum alloy containing substantially no silicon.

10. The semiconductor integrated circuit according to claim 7, wherein a contour of the contact hole and a head of the insulator region are tapered.

11. The semiconductor integrated circuit according to claim 7, wherein the columnar insulator region in the contact hole is connected to the interlayer insulating film at at least one sidewall of the contact hole.

12. The semiconductor integrated circuit according to claim 7, wherein:

the semiconductor substrate further has a second device formed in a second semiconductor region on or over the surface of the semiconductor substrate;

the interlayer insulating film further has a second contact hole over the second semiconductor region, the second contact hole being filled with a plug; and

the electrode further includes a second electrode that contacts the second semiconductor region via the plug.

13. The semiconductor integrated circuit according to claim 7, wherein, within the contact hole, a ratio of an area where the insulator region does not exist to a total area of the bottom of the contact hole is within a range of from about 0.2 to about 0.5.

14. A method of manufacturing a semiconductor integrated circuit comprising:

providing a semiconductor substrate having a fuse device present at least partly in a semiconductor region on or over a surface of the semiconductor substrate;

forming an interlayer insulating film over the surface of the semiconductor substrate, the interlayer insulating film having a top surface;

forming a contact hole in the interlayer insulating film over the semiconductor region; and

forming a film of an electrode material in the contact hole to form an electrode that contacts the semiconductor region at a bottom of the contact hole,

wherein the forming of the contact hole and the forming of the film of electrode material in the contact hole further includes:

reducing a contact area between the electrode and the semiconductor region by forming a columnar insulator region at a central portion of the contact hole; and

increasing an amount of the electrode material in the contact hole by making a top end of the columnar insulator region lower than the top surface of the interlayer insulating film.

15. The method according to claim 14, wherein the forming of the film of electrode material in the contact hole further includes further increasing the amount of electrode material in the contact hole by tapering a head of the insulator region and a contour of the contact hole.

16. The method according to claim 14, wherein, within the contact hole, a ratio of an area where the insulator region does not exist to a total area of the bottom of the contact hole is within a range of from about 0.2 to about 0.5.